ABSTRACT OF THE DISCLOSURE

A software simulation technique for pipelined hardware is provided in which the hardware is modelled as a plurality of pipelined circuit element models that each respectively read their input data values from a first data storage area A and write their output data values to a second data storage area B. At the end of each simulated clock signal cycle, the first data storage area A and the second data storage area B are swapped to effectively replicate the behaviour of the passing of signal values between pipelined stages in a hardware pipeline.

[Figure 2]